IN THE CLAIMS:

1. (CURRENTLY AMENDED) A system configured to acknowledge ~~provide fast acknowledgement~~ and ~~efficient servicing~~ service ~~of~~ an interrupt issued to a processor of an intermediate node, the system comprising:

an external device coupled to a high latency path, the external device generating a pulsed interrupt signal for each type of interrupt supported by the processor;

an interrupt multiplexing device accessible by the processor over a fast bus, the interrupt multiplexing device adapted to issue the interrupt to the processor in response to each pulsed interrupt signal generated by the external device;

a low latency path coupling the external device to the interrupt multiplexing device and adapted to transport each pulsed interrupt signal generated by the external device to the interrupt multiplexing device; and

a status bit stored within the interrupt multiplexing device, the status bit adapted for assertion whenever the pulsed interrupt signal is detected at the interrupt multiplexing device,

wherein the processor efficiently acknowledges the issued interrupt by accessing the interrupt multiplexing device over the fast bus.

2. (ORIGINAL) The system of Claim 1 further comprising a current counter associated with the interrupt multiplexing device, the current counter incremented in response to each pulsed interrupt signal at the interrupt multiplexing device.

3. (ORIGINAL) The system of Claim 2 further comprising an interrupt handler invoked by the processor to service the issued interrupt.

4. (ORIGINAL) The system of Claim 3 further comprising a last counter associated with the processor, the last counter incremented in response to each interrupt serviced by the CPU.

5. (ORIGINAL) The system of Claim 4 further comprising means for comparing a value of the last counter with a value of the current counter to determine whether there are more interrupts to service.

6. (ORIGINAL) The system of Claim 5 wherein the means for comparing comprises the interrupt handler.

7. (ORIGINAL) The system of Claim 1 wherein the external device is a direct memory access controller.

8. (ORIGINAL) The system of Claim 1 wherein the low latency path is a printed circuit board trace.

9. (ORIGINAL) The system of Claim 1 wherein the high latency path is a peripheral computer interconnect bus.

10. (ORIGINAL) The system of Claim 1 wherein the interrupt multiplexing device is a field programmable gate array device.

11. (CURRENTLY AMENDED) A method for ~~providing fast acknowledgement~~ acknowledging and ~~efficient~~ servicing ~~of~~ an interrupt issued to a processor of an intermediate node, the method comprising the steps of:

generating a pulsed interrupt signal at an external device coupled to a high latency path;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

invoking an interrupt handler to service the issued interrupt.

12. (CURRENTLY AMENDED) The method of Claim 11 further comprising the steps of:

initializing a last counter; and

incrementing the last counter in response to each interrupt serviced.

13. (ORIGINAL) The method of Claim 12 further comprising the steps of:

reading the status bit; and

if the status bit is clear, dismissing the handler.

14. (ORIGINAL) The method of Claim 13 wherein the step of reading further comprises the step of clearing the status bit.

15. (CURRENTLY AMENDED) The method of Claim 13 further comprising the steps of:

incrementing a current counter in response to each pulsed interrupt signal at the interrupt multiplexing device;

if the status bit is set, reading a value of ~~a~~ the current counter;

comparing the current counter value with a value of the last counter; and

if the last counter value is greater than or equal to the current counter value, returning to the step of reading the status bit.

16. (ORIGINAL) The method of Claim 15 further comprising the steps of:

if the last counter value is not greater than or equal to the current counter value, checking a control block stored in a memory of the node, the control block shared between the processor and the external device; and

determining whether the processor owns the control block.

17. (ORIGINAL) The method of Claim 16 further comprising the steps of:

if the processor owns the control block, processing the control block; and

incrementing the last counter.

18. (ORIGINAL) The method of Claim 17 further comprising the steps of:

determining whether a preset limit for processing control blocks has been reached; and

if the preset limit is reached, dismissing the handler.

19. (CURRENTLY AMENDED) Apparatus for ~~providing fast acknowledgement~~ acknolwedging and ~~efficient~~ servicing ~~of~~ an interrupt issued to a processor of an intermediate node, the apparatus comprising:

means for generating a pulsed interrupt signal at an external device coupled to a high latency path;

means for transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

means for asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

means for issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

means for invoking an interrupt handler to service the issued interrupt.

20. (ORIGINAL) A computer readable medium containing executable program instructions for ~~providing fast acknowledgement~~ acknowledging and ~~efficient~~ servicing ~~of~~ an interrupt issued to a processor of an intermediate node, the executable program instructions comprising program instructions for:

generating a pulsed interrupt signal at an external device coupled to a high latency path;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

invoking an interrupt handler to service the issued interrupt.

21. (NEW) Electromagnetic signals propagating on a computer network comprising, the electromagnetic signals carrying instructions for execution on a processor for:

generating a pulsed interrupt signal at an external device coupled to a high latency path;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a low latency path coupling the external device to the interrupt multiplexing device;

asserting a status bit in response to detecting the pulsed interrupt signal at the interrupt multiplexing device;

issuing the interrupt to the processor in response to each pulsed interrupt signal received at the interrupt multiplexing device; and

invoking an interrupt handler to service the issued interrupt.

22. (NEW) A method for acknowledging and servicing an interrupt issued to a processor, the method comprising:

generating a pulsed interrupt signal at an external device;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device;

asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;

issuing the interrupt to the processor over a second low latency path;

reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.

23. (NEW) The method of claim 22 further comprising:

checking, by the interrupt handler, ownership of a control block and in response to the processor owning the control block, processing the control block.

24. (NEW) The method of claim 23 further comprising:

assigning ownership of the control block over a high latency path.

25. (NEW) The method of claim 23 further comprising:

incrementing a current counter in response to each pulsed interrupt signal received at the interrupt multiplexing device;

incrementing a last counter in response each control block processed by the interrupt handler;

comparing the value of the current counter and the value of the last counter; and

if the value of the current counter is greater than the value of the last counter, which thereby indicates the control block corresponding to the interrupt has not yet been processed, continuing to attempt to access and process the control block.

26. (NEW) The method of Claim 25 further comprising:

determining whether a preset limit for processing control blocks has been reached; and

if the preset limit is reached, dismissing the interrupt handler.

27. (NEW) An apparatus for acknowledging and servicing an interrupt issued to a processor, the apparatus comprising:

an external device generating a pulsed interrupt signal;

a first low latency path that couples the external device to and interrupt multiplexing device for transporting the pulsed interrupt signal to the interrupt multiplexing device;

a status bit in the interrupt multiplexing device corresponding to the asserted interrupt and set in response to detecting the pulsed interrupt signal;

a second low latency path for issuing the interrupt to the processor;

an interrupt handler internal to the processor for reading the status bit over the second low latency path, where the status bit is cleared in response the reading to effectively acknowledge the interrupt.

28. (NEW) The apparatus of claim 27 further comprising:

the interrupt handler checks ownership of a control block and, in response to the processor owning the control block, processes the control block.

29. (NEW) The apparatus of claim 28 further comprising:

a high latency path through which ownership of the control block is assigned.

30. (NEW) The apparatus of claim 28 further comprising:

a current counter incremented in response to each pulsed interrupt signal received at the interrupt multiplexing device;

a last counter incremented in response to each control block processed by the interrupt handler; and

a comparator for comparing the value of the current counter and the value of the last counter and if the value of the current counter is greater than the value of the last counter, which thereby indicates the control block corresponding to the interrupt has not yet been processed.

31. (NEW) The apparatus of Claim 30 further comprising:

circuitry for determining whether a preset limit for processing control blocks has been reached a for dismissing the interrupt handler if the preset limit is reached.

32. (NEW) An apparatus for acknowledging and servicing an interrupt issued to a processor, the apparatus comprising:

means for generating a pulsed interrupt signal at an external device;

means for transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device;

means for asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;

means for issuing the interrupt to the processor over a second low latency path;

means for reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

means for clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.

33. (NEW) A computer readable media comprising, the computer readable media having instructions written thereon for execution on a processor for:

generating a pulsed interrupt signal at an external device;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device;

asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;

issuing the interrupt to the processor over a second low latency path;

reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.

34. (NEW) Electromagnetic signals propagating on a computer network comprising, the electromagnetic signals carrying instructions for execution on a processor for:

generating a pulsed interrupt signal at an external device;

transporting the pulsed interrupt signal to an interrupt multiplexing device over a first low latency path that couples the external device to the interrupt multiplexing device;

asserting a status bit in the interrupt multiplexing device corresponding to the interrupt in response to detecting the pulsed interrupt signal;

issuing the interrupt to the processor over a second low latency path;

reading the status bit over the second low latency path by an interrupt handler internal to the processor; and

clearing the status bit in response to the reading of the status bit to effectively acknowledge the interrupt.